REMARKS

Claims 19-28, 30-37 and 39-41 are pending in this application. Claims 19-25, 30-34, 39 and 40 have been amended. Claims 29 and 38 have been canceled.

The drawings stand objected to because "Figures 1-3 should be designated by a legend such as -- Prior Art-- ." (Office Action at 2). Applicants are submitting concurrently herewith a proposed drawing amendment for Figures 1-3 for the Examiner's approval. Each of Figures 1-3 is labeled --Prior Art--. Applicants respectfully submit that the corrections to Figures 1-3 obviate the Examiner's objection.

Claims 19-25, 28, 30-34, 37 and 39-41 stand rejected under stand 35 U.S.C. §103(a) as being unpatentable over Colgan et al. (U.S. Patent No. 5,565,707) ("Colgan") in view of Venkatraman et al. (U.S. Patent No. 6,093,966) ("Venkatraman"). The rejection is respectfully traversed.

The claimed invention relates to a dual damascene structure comprising a titanium-silicon-nitride layer. As such, amended independent claim 19 recites a "dual damascene structure" comprising *inter alia* a metal layer "provided within" a first insulating layer, "a second insulating layer provided over said metal layer" and "a via situated within said second insulating layer and . . . lined with a titanium-silicon-nitride layer and filled with a copper material." Amended independent claim 19 also recites a trench situated within a third insulating layer and "lined with said titanium-silicon-nitride layer and filled with said copper material."

Amended independent claim 31 recites a "damascene structure" comprising *inter alia* a semiconductor substrate, "a metal layer provided within" a first insulating layer and "at least another insulating layer provided over said metal layer." Amended independent claim 31 also recites "at least one opening situated within said at least another insulating layer and . . . lined with a titanium-silicon-nitride layer and filled with a copper material." Amended independent claim 40 recites "a damascene structure" which is part of

a processor-based system and which comprises *inter alia* "a metal layer provided within a first insulating layer" and "at least another insulating layer provided over said metal layer." Amended independent claim 40 also recites "at least one opening situated within said at least another insulating layer and . . . lined with a titanium-silicon-nitride layer and filled with copper."

Colgan relates to an interconnect structure comprising interlayer contact regions or studs. (Abstract; Title). According to Colgan, interlayer contact regions or studs 12, 13 are provided between patterned interconnect layers 30, 40 to "overcome[s] the problem of electromigration at high current density" which occurs in interconnect structures of integrated circuit chips. (Abstract; Figure 1). Colgan teaches that the interlayer contact regions or studs 12, 13 comprise "substantially the compound Al_2Cu in the theta phase." (Col. 4, lines 8-9). Colgan also teaches that the interconnect layers 30, 40 comprise a "metal selected from the group consisting of copper, copper alloys, aluminum and aluminum alloys." (Col. 4, lines 36-40).

Venkatraman relates to an interconnect structure comprising a copper barrier layer that prevents silicon enrichment at the bottom of such structure. (Abstract; Col. 12-16). Venkatraman teaches openings 195, 196 formed within a first and second insulating layers 180, 190 and provided with copper barrier layers 200, 201 having different silicon concentrations. (Abstract; Figures 9-10). Venkatraman notes that copper barrier layer 200 (201) "is typically a tantalum silicon nitride layer, but may also be composed of any combination of refractory metal such as molybdenum, tungsten, titanium, vanadium together with silicon and nitrogen (e.g. a nitrogen-containing tantalum)." (Col. 5, lines 22-27).

The subject matter of claims 19-25, 28, 30-34, 37 and 39-41 would not have been obvious over Colgan in view of Venkatraman. Indeed, the Office Action fails to establish a *prima facie* case of obviousness. Courts have generally recognized that a showing of a *prima facie* case of obviousness necessitates three requirements: (i) some suggestion or motivation, either in the references themselves or in the knowledge of a

person of ordinary skill in the art, to modify the reference or combine the reference teachings; (ii) a reasonable expectation of success; and (iii) the prior art references must teach or suggest all claim limitations. See e.g., In re Dembiczak, 175 F.3d 994, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999); In re Rouffet, 149 F.3d 1350, 1355, 47 U.S.P.Q.2d 1453, 1456 (Fed. Cir. 1998); Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc., 75 F.3d 1568, 1573, 37 U.S.P.Q.2d 1626, 1630 (Fed. Cir. 1996).

In the present case, neither Colgan nor Venkatraman, whether considered alone or in combination, teaches or suggests the limitations of claims 19-25, 28, 30-34, 37 and 39-41. Colgan fails to teach or suggest a "dual damascene structure," much less a dual damascene structure comprising "a via situated within said second insulating layer and . . . lined with a titanium-silicon-nitride layer and filled with a copper material," as amended independent claim 19 recites. Colgan also fails to teach or suggest a trench "extending to said via" and "lined with said titanium-silicon-nitride layer and filled with said copper material," as amended independent claim 19 further recites. As noted above, Colgan teaches studs 12, 13 comprising "substantially the compound Al_2Cu in the theta phase" provided between patterned interconnect layers 30, 40 (col. 4, lines 8-9), and not a dual damascene structure, as in the claimed invention.

Colgan is also silent about a "damascene structure," much less about a damascene structure comprising "at least one opening . . . lined with a titanium-silicon-nitride layer and filled with copper," as amended independent claims 31 and 40 recite. Colgan teaches Al_2Cu studs 12, 13 which are not lined with any material, much less with "a titanium-silicon-nitride layer and filled with copper," as in the claimed invention.

Similarly, Venkatraman does not teach or suggest all limitations of amended independent claims 19, 31 and 40. Venkatraman fails to teach or suggest a "damascene structure" comprising a substrate and "a via" (claim 19) or "at least one opening" (claims 31, 40) situated over "a metal layer provided within a first insulating layer," as amended independent claims 19, 31 and 40 recite. Venkatraman teaches openings 195, 196 formed within a first and second insulating layers 180, 190 and provided with copper barrier layers

200, 201 having different silicon concentrations. (Abstract; Figures 9-10). In Venkatraman, however, metal layer 170 is not provided within an insulating layer, as in the claimed invention.

In addition, a person of ordinary skill in the art would not have been motivated to combine the teachings of Colgan with those of Venkatraman because no suggestion or motivation to combine the references exists. Courts have generally held that, to establish a *prima facie* case of obviousness, "[I]t is insufficient that the prior art disclosed the components of the patented device, either separately or used in other combinations; there must be some teaching, suggestion, or incentive to make the combination made by the inventor." Northern Telecom, Inc. v. Datapoint Corp., 908 F.2d 931, 934, 15 U.S.P.Q.2d 1321, 1323 (Fed. Cir. 1990). This way, "the inquiry is not whether each element existed in the prior art, but whether the prior art made obvious the invention as a whole for which patentability is claimed." Hartness Int'l, Inc. v. Simplimatic Engineering Co., 819 F.2d 1100, 1108, 2 U.S.P.Q.2d 1826, 1832 (Fed. Cir. 1987). Accordingly, a determination of obviousness "must involve more than indiscriminately combining prior art; a motivation or suggestion to combine must exist." Pro-Mold & Tool Co., 75 F.3d at 1573.

The crux of Colgan is "resisting electromigration" in an integrated circuit chip by "incorporating patterned interconnect layers of Al or Al-Cu and interlayer contact regions or studs of Al_2Cu between patterned interconnect layers." (Abstract). This way, Colgan "overcomes the problem of electromigration at high current density in the interconnect structure by providing a continuous path for Cu and/or Al atoms to move in the interconnect structure." (Abstract). In contrast, the crux of Venkatraman is the elimination of "silicon enrichment at the bottom of the trench that may cause device failure." (Col. 1, lines 64-67). For this, Venkatraman teaches two copper barrier layers 200, 201 which are formed at different stage bias so that the silicon concentration of the copper barrier layers located at the bottom of the trench is much lower (less than 5%) than the silicon concentration of the copper barrier layers located on the sidewalls of the trench

(in the range of 10-20%). (Col. 6, lines 46-48). Thus, one skilled in the art would not have been motivated to combine Venkatraman, which teaches a copper barrier layer between a metal interconnect layer and a damascene structure for preventing silicon enrichment, with Colgan, which teaches against the use of a barrier layer between the Al or Cu interconnect layer 30 and the Al_2Cu studs 12, 24 to provide a continuous path for the Al and/or Cu atoms. In view of the above, the subject matter of claims 19-25, 28, 30-34, 37 and 39-41 would not have been obvious over Colgan in view of Venkatraman, and withdrawal of the rejection of these claims is respectfully requested.

Claims 26, 27, 35 and 36 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Colgan et al. (U.S. Patent No. 5,565,707) ("Colgan") and Venkatraman et al. (U.S. Patent No. 6,093,966) ("Venkatraman") in further view of *Ti-Si-N Diffusion Barriers Between Silicon and Copper* by J.S. Reid et al. ("Reid"). The rejection is respectfully traversed.

Reid teaches a 10nm (100 Angstroms) titanium silicon nitrogen barrier layer between a silicon substrate and a copper overlayer. Because none of Colgan, Venkatraman and Reid teaches or suggests the limitations of amended independent claims 19, 31 and 40, the subject matter of claims 26, 27, 35 and 36 would not have been obvious over Colgan and Venkatraman in view of Reid, and withdrawal of the rejection of these claims is also respectfully requested.

A marked-up version of the changes made to the specification and claims by the current amendment is attached. The attached page is captioned "**Version with markings to show changes made.**"

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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Version With Markings to Show Changes Made

19. (amended) A dual damascene structure comprising:

a semiconductor substrate;

a first insulating layer provided over said semiconductor substrate;

a metal layer provided within said [substrate] first insulating layer;

a [first] second insulating layer [located] provided over said [substrate] metal layer;

a via situated within said [first] second insulating layer and extending to at least a portion of said metal layer, said via being lined with a titanium-silicon-nitride layer and filled with a copper material;

a [second] third insulating layer located over said [first] second insulating layer;

a trench situated within said [second] third insulating layer and extending to said via, said trench being lined with said titanium-silicon-nitride layer and filled with said copper material.

20. (amended) The dual damascene structure of claim 19, wherein said [first] second insulating layer includes a material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS.

21. (amended) The dual damascene structure of claim 19, wherein said [first] second insulating layer includes silicon dioxide.

22. (amended) The dual damascene structure of claim 19, wherein said [first] second insulating layer has a thickness of about 2,000 to 15,000 Angstroms.

23. (amended) The dual damascene structure of claim 19, wherein said [second] third insulating layer includes a material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS.

24. (amended) The dual damascene structure of claim 19, wherein said [second] third insulating layer includes silicon dioxide.

25. (amended) The dual damascene structure of claim 19, wherein said [second] third insulating layer has a thickness of about 2,000 to 15,000 Angstroms.

30. (amended) The dual damascene structure of claim [29] 19, wherein said substrate is a silicon substrate.

31. (amended) A damascene structure comprising:

a semiconductor substrate;

a first insulating layer provided over said semiconductor substrate;

a metal layer provided within said [substrate] first insulating layer;

at least [one] another insulating layer [located] provided over said [substrate] metal layer; and

at least one opening situated within said at least [one] another insulating layer and extending to at least a portion of said metal layer, said opening being lined with a titanium-silicon-nitride layer and filled with a copper material[;].

32. (amended) The damascene structure of claim 31, wherein said at least [one] another insulating layer includes a material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS.

33. (amended) The damascene structure of claim 31, wherein said at least [one] another insulating layer includes silicon dioxide.

34. (amended) The damascene structure of claim 31, wherein said at least [one] another insulating layer has a thickness of about 2,000 to 15,000 Angstroms.

39. (amended) The damascene structure of claim [38] 31, wherein said substrate is a silicon substrate.

40. (amended) A processor-based system comprising:

a processor; and

an integrated circuit coupled to said processor, at least one of said processor and integrated circuit including a damascene structure, said damascene structure comprising a metal layer [over] provided within a first insulating layer formed over a substrate, at least [one] another insulating layer [located] provided over said metal layer, and at least one opening situated within said at least [one] another insulating

layer and extending to at least a portion of said metal layer, said opening being lined with a titanium-silicon-nitride layer and filled with copper.